EXHIBIT 8

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., **Plaintiff,** **vs.** **MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; AND MICRON TECHNOLOGY TEXAS LLC,** **Defendants.**	**Civil Action No. 2:22-cv-203-JRG**

DECLARATION OF HAROLD S. STONE, PH.D.,
IN SUPPORT OF DEFENDANTS' CLAIM CONSTRUCTION POSITIONS

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I, Harold S. Stone, hereby declare as follows:

I. INTRODUCTION

1. My name is Harold S. Stone, Ph.D. I have prepared this declaration as an expert witness on behalf of Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively, "Micron" or "Defendants"), in this lawsuit with Plaintiff Netlist Inc. ("Netlist"), to provide my analyses and opinions in certain technical aspects of this dispute. In this declaration, I give my analysis and opinions about how a person of ordinary skill in the art at the time of the alleged inventions would have understood certain claim terms in U.S. Patent Nos. 8,787,060 (the "'060 patent"), 9,318,160 (the "'160 patent"), 11,016,918 (the "'918 patent"), and 11,232,054 (the "'054 patent") (collectively, the "Asserted Patents").

2. This declaration contains statements of my opinions formed to date, and the bases and rationale for these opinions. To the extent Netlist produces one or more expert declarations supporting its positions, I reserve the right to supplement or amend my opinions here upon reviewing such declaration(s). At this time, I have only set forth opinions below as to a subset of the claim terms in dispute. However, I reserve the right to respond to any arguments by Netlist's experts regarding the claim terms, including claim terms for which I have not provided an opinion herein.

3. I provide information helpful to the Court in understanding how a person of ordinary skill in the art (a "POSITA") would have understood each claim term at the time of the claimed priority date for the respective patents. For example, for certain terms, my declaration may focus on the understanding of a POSITA in light of textbooks and dictionary definitions, whereas for other terms, my declaration may focus on the understanding of a POSITA in the context of the claims in which the claim terms appear. However, for each claim term, I reserve the right to supplement or amend my opinions to provide further explanation regarding why additional

intrinsic and extrinsic evidence supports a construction, as necessary to respond to Netlist's experts.

4. I am being compensated for the time I have spent on this litigation at my customary rate of $500 per hour. My compensation does not depend in any way upon the opinions I provide or the outcome of this litigation.

II. BACKGROUND AND QUALIFICATIONS

5. Exhibit A is a true and correct copy of my *Curriculum Vitae* describing my background and experience. My qualifications generally are set forth in that exhibit. It also includes a list of the publications I have authored and a list of the other cases in which I have testified. I have personal knowledge of the facts and opinions set forth in this declaration, and, if called upon to do so, I would testify competently thereto.

6. I was awarded a Ph.D. and master's degree in Electrical Engineering from the University of California-Berkeley in 1963 and 1961, respectively. I received a Bachelor of Science degree in Electrical Engineering from Princeton University in 1960.

7. After my graduation from Berkeley in 1963, I served as a Research Engineer at Boeing and SRI International. I then held faculty positions at Stanford University and at the University of Massachusetts, where I served as a professor of computer science and electrical engineering.

8. In 1977, together with W. Kahan and J. Coonen, I authored the original proposal (the "KCS proposal") to the working group charged for developing a floating-point standard, which is now known as the IEEE 754 Floating Point Standard. The standard that emerged is that proposal with small changes and additions. It has been implemented in several billion processors.

9. In 1984, I started working for IBM as a Manager of Advanced Architecture Studies. In 1990, I became a Research Staff Member at IBM. During my time at IBM, I managed and

conducted research in the area of memory systems and optical interconnections. I worked at IBM until 1994, when I became a Fellow at the NEC Research Institute, the highest technical position in the company. At NEC, I conducted research in image processing. I am an inventor of a patent to NEC regarding a technique for decompressing JPEG images in a novel way that permits images to be searched without fully decompressing them. The decompression technique is based on inverse discrete cosine transforms, which are one of the basic elements of MPEG decompression.

10. I have authored, coauthored, or edited nine books in various technical areas, the most recent of which appeared in 2011. My textbooks have sold over 100,000 copies. My work on the use of the perfect shuffle interconnections for supercomputers is widely recognized, and many supercomputers based on these interconnections were developed and marketed. For this work and my textbook contributions to the field, I was elected an IEEE Fellow and ACM Fellow, and received the IEEE Piore Field Award, the IEEE Computer Society Taylor Booth Award, and the Charles Babbage Award. I am the principal inventor or co-inventor of 27 patents, including seven in the area of computer architecture: U.S. Patent Nos. 4,989,131; 5,065,310; 5,163,149; 5,611,070; 5,742,785; 5,790,823; and 6,311,260.

11. I have served as a consultant to industry while holding my academic positions and have extensive experience in computer design for embedded computers as a consequence, including low-power computers for use in satellites and ultra-reliable computers for use in nuclear submarine navigation systems. In recent years, I have been a member of two Division Review Committees at Los Alamos National Laboratory in the area of Nuclear Nonproliferation and a consultant to NASA in the area of satellite image processing.

III. MATERIALS CONSIDERED

12. As part of my preparation for writing this declaration, I reviewed the Asserted Patents, their prosecution histories (including their provisional applications), the parties' proposed constructions, and respective identification of extrinsic evidence.

IV. APPLICABLE LEGAL STANDARDS

13. I am not a patent attorney and do not have any formal legal training. I will not offer opinions on the law. I have been informed by counsel regarding the applicable legal standards for claim construction, as described in this section. I have relied on these principles in forming my opinions.

A. Claim Construction

14. I have been instructed by counsel on the law regarding claim construction and patent claims and understand that a patent may include two types of claims: independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim or another dependent claim. I understand that a dependent claim includes all the limitations that it recites in addition to all of the limitations recited in the claim from which it depends.

15. I understand that claim construction is a matter of law and will be decided by the Court. It is my understanding that in proceedings before the district court, claim terms are given the ordinary and customary meaning the terms would have to a POSITA at the time of the invention, in view of the patent specification and file history, in the context of the particular claim in which it appears, as well as in light of any other relevant evidence intrinsic and extrinsic to the patent. Intrinsic evidence includes the patent and its prosecution history. Extrinsic evidence is all evidence external to the patent and prosecution history, such as expert or inventor testimony or dictionaries. I am informed that 35 U.S.C. § 112 is applicable law and states, "[t]he specification

shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention."

B. Indefiniteness

16. I understand that a claim is invalid for indefiniteness if the claim, read in light of the specification and the prosecution history, fails to inform, with reasonable certainty, those skilled in the art about the scope of the invention. I understand the test for indefiniteness is met where a POSITA cannot ascertain the boundary of the claim with reasonable certainty. This may occur, for example, when subjective terms of degree are used in a claim such that a POSITA has no objective guide to distinguish subject matter that practices or teaches the claim from subject matter that does not. Similarly, measurements or assessments used in a claim without a clear indication of how those measurements or assessments may be made would leave a POSITA unable to objectively determine the boundary of the claim and render that claim indefinite.

C. Means-Plus-Function Terms

17. In addition to claim terms construed according to the principles discussed above, I understand that 35 U.S.C. § 112 of the patent laws allows patent claims to include limitations expressed as a means for performing a specified function without reciting structure or material for performing that function. I further understand that when this technique is used, such a claim term shall not be construed to cover every conceivable structure for performing the specified function, but rather is construed to cover the structure clearly linked to the function in the patent specification and equivalents thereof. This, I understand, is to avoid claims that are expressed in purely functional terms and are unbounded by any reference to structure in the specification.

18. I understand that a solely functional claim term can include the word "means," and there is a presumption against solely functional claiming in the absence of "means." I further understand a claim limitation lacking the word "means" may also still be a solely functional claim

term if the claim fails to recite sufficiently definite structure or else recites function without reciting sufficient structure for performing that function. Thus, if a POSITA understands the words of the claim as lacking a sufficiently definite meaning as a name for structure for performing the specified function, the term is solely functional, and it must be construed to cover the structure clearly linked to the specified function described in the patent specification. For instance, I understand that generic terms such as "module," "mechanism," "element," and "device" are words that can, depending on the circumstances, operate as substitutes for "means" in a solely functional claim term because they typically do not denote sufficiently definite structure for the claimed function. Thus, in construing claim terms, I understand that a threshold question is whether the term is a solely functional term. Using the traditional tools of claim construction I discussed above—including considering the use of the term, if any, in the specification and prosecution history—I understand that one must inquire as to whether a claim term denotes a definite structure in the particular context of the claim. If it does so, then the term is not a solely functional claim term.

19. If, on the other hand, a claim term is determined to be solely functional, I understand that it must be construed through a further two-step process. First, the claimed function must be identified. Next, it must be determined what structure, if any, is clearly linked in the specification to performance of the claimed function. I understand that even if the specification discloses corresponding structure, the disclosure must be of "adequate" corresponding structure to achieve the claimed function. I understand that if a POSITA would be unable to recognize the structure in the specification and a clear link with the corresponding function in the claim, a solely functional claim term is indefinite.

V. PERSON OF ORDINARY SKILL IN THE ART

20. I understand that a person of ordinary skill in the art (a "POSITA") is a hypothetical person who is presumed to be familiar with the relevant field and its literature at the time of the

inventions. I further understand that a POSITA is also a person of ordinary creativity, capable of understanding the scientific principles applicable to the pertinent field. I also understand that in determining the level of ordinary skill in the art of a POSITA, I may consider, among other things, the types of problems encountered in the field, prior solutions to those problems, how quickly innovations are made in the field, the sophistication of the technology, and the levels of education and experience of persons working in the field. I understand that a POSITA is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors above.

21. For each of the Asserted Patents, I use the term "POSITA" to refer to a person with the qualifications described below or similar qualifications. To have similar qualifications, an individual with additional education or additional industrial experience could still be of ordinary skill in the art if that additional aspect compensates for a deficit in one of the other aspects of the requirements stated below.

22. The basis for my familiarity with the level of ordinary skill is my interaction with large numbers of students seeking related technical degrees over many years of teaching, and with people working in the relevant disciplines who were at this level of skill. In reaching this opinion, I have considered the types of problems encountered in the art, the prior art solutions to those problems, the speed with which innovations are made, the maturity of the relevant technology, and the educational and professional levels of people working in the field. In addition, I believe that at the time of the purported invention for each Asserted Patent, I would have qualified as a person of ordinary skill in the art pertaining to the Asserted Patents.

A. '060 and '160 patents

23. In my opinion, a POSITA in the field of the '060 and '160 patents at the time of the claimed inventions of the '060 and '160 patents would have had have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the

field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of DRAM and SDRAM memory devices and memory modules, including standardized interfaces for interfacing with a memory controller and other parts of a computer system. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used in stacked memory devices, including structure and circuitry in JEDEC-proposed three-dimensional stacking and circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers and their corresponding electrical loads.

24. My opinions that relate to the '060 and '160 patents are based on the asserted priority date of November 3, 2010. In the parts of this declaration that relate to the '060 and '160 patents, a POSITA would have had the requisite education and/or experience by November 3, 2010. In this declaration, I offer no opinion or analysis about whether the asserted priority date for the '060 and '160 patents is correct.

B. '918 and '054 patents

25. In my opinion, a POSITA in the field of the '918 and '054 patents at the time of the claimed inventions of the '918 and '054 patents would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and

SDRAM memory devices and memory modules and how they interacted with a memory controller and other parts of a computer system, including standard communication busses and protocols, such as PCI and SMBus busses and protocols. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers. Such a hypothetical person would further have been familiar with voltage supply requirements of such structures (e.g., memory modules, memory devices, memory controllers, and associated access and control circuitry), including voltage conversion and voltage regulation circuitry.

26. My opinions that relate to the ’918 and ’054 patents are based on the asserted priority date of June 1, 2007. In the parts of this declaration that relate to the ’918 and ’054 patents, a POSITA would have had the requisite education and/or experience by June 1, 2007. In this declaration, I offer no opinion or analysis about whether the asserted June 1, 2007 priority date for the ’918 and ’054 patents is correct.

VI. OVERVIEW OF THE PATENTS AND RELATED TECHNOLOGY

A. ’060 and ’160 patents

27. The ’060 and ’160 Patents all claim priority to the same provisional applications and share a common specification. Therefore, I will cite to one patent for ease of reference but the citation can be found in both patents.

28. The ’060 and ’160 Patents state that they “relate[] to systems and methods for reducing the load of drivers of memory packages.” ’060 Patent at 1:19-21. The ’060 and ’160 Patents admit as prior art “FIGS. 1A and 1B [which] schematically illustrate examples of existing memory package designs currently used or proposed to be used.” *Id*. at 1:30-33 and Fig. 1B (reproduced below, annotated).

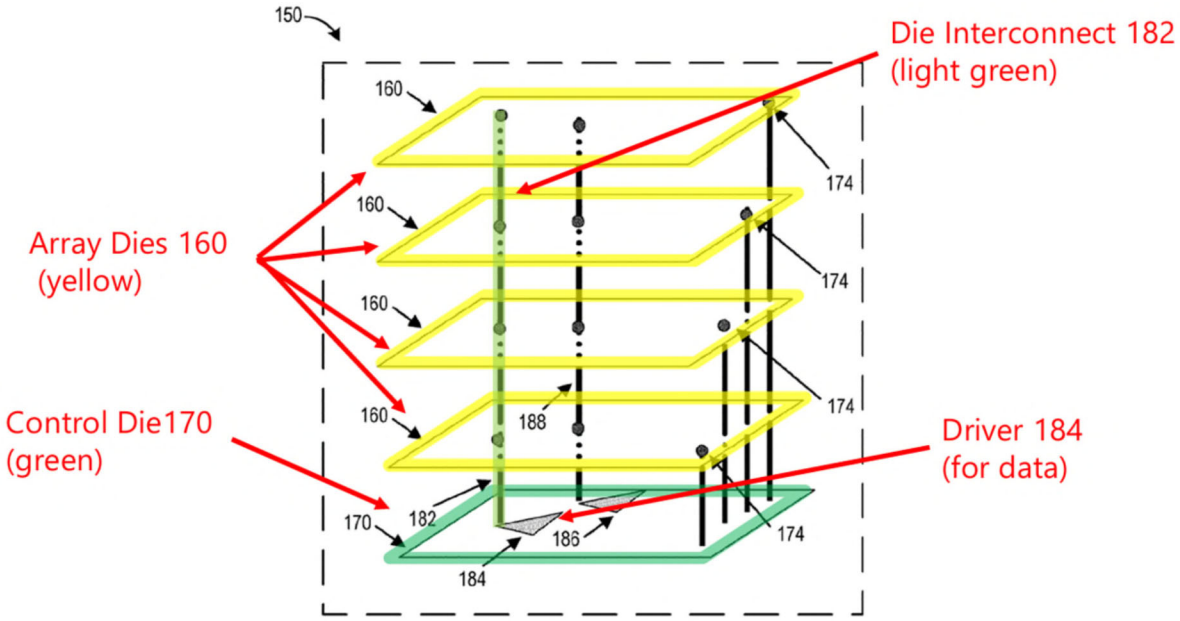
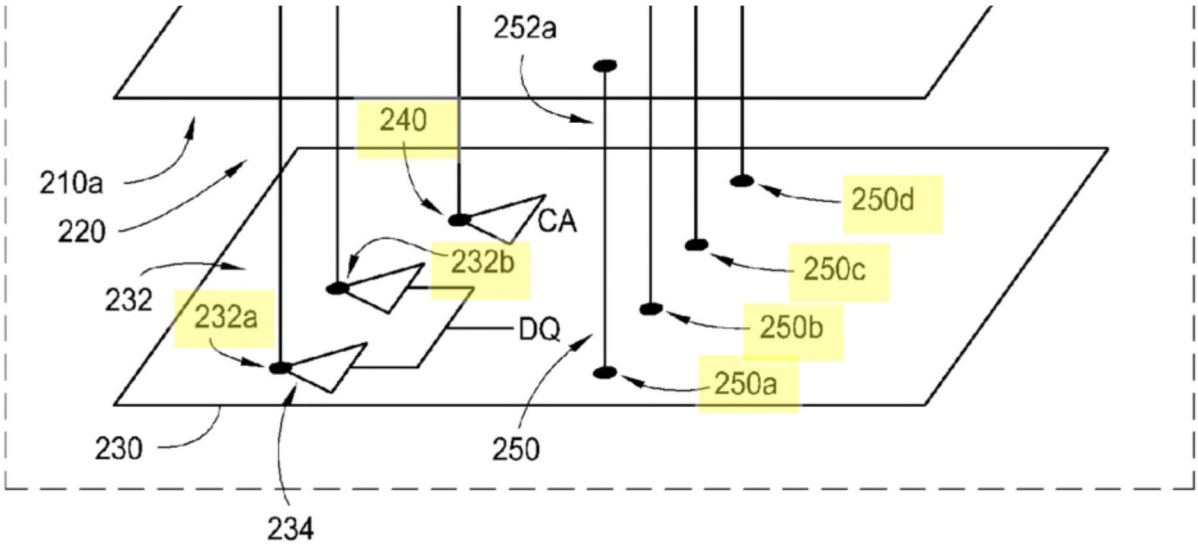


FIG. 1B

29. In particular, "FIG. 1B schematically illustrates an example of a memory package 150 that includes four array dies 160 [(yellow)] and a control die 170 [(green)] that … [includes] a driver 184 that drives data signals to each of the array dies 160 along a corresponding die interconnect 182." '060 Patent at 1:63-2:4. The '060 and '160 Patents explain that a problem with the prior-art memory package is that the data driver 184 has to drive a load that is "in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies. Thus, to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power." *Id*. at 2:8-15.

30. The '060 and '160 Patents disclose that each die interconnect has a corresponding "conduit" which is configured to transmit a signal to the die interconnect. '060 Patent at Fig. 2 (reproduced below in part, annotated, showing data conduits 232a and 232b, command/address conduits 240, and chip select conduits 250a-d), 6:48-59 (describing data conduits 232a and 232b),

9:28-60 (describing command/address conduits 240 and chip select conduits 250). A "conduit" may, but does not have to, include a driver to drive the load on the conduit. *Id.*; *see also* 6:60-62 ("In some embodiments, the data conduits 232 may also include one or more drivers 234 as schematically illustrated by FIG. 2."), 21:18-20 ("The command/address bus 814, although illustrated as a single line, may include as many lines or signal conduits as the number of bits of the command/address signal.").



31. The '060 and '160 Patents solve the prior art's problem of having too much load on the data conduits by replacing one data driver of the prior art with two (or more) drivers 234 coupled to the same DQ data terminal, each of the drivers driving the data signal through a respective die interconnect (220a, 220b) that is in electrical communication with a subset of the array dies, thus reducing the overall load of each data conduit. '060 Patent at 7:9-8:18 and Fig. 2 (reproduced below, annotated).

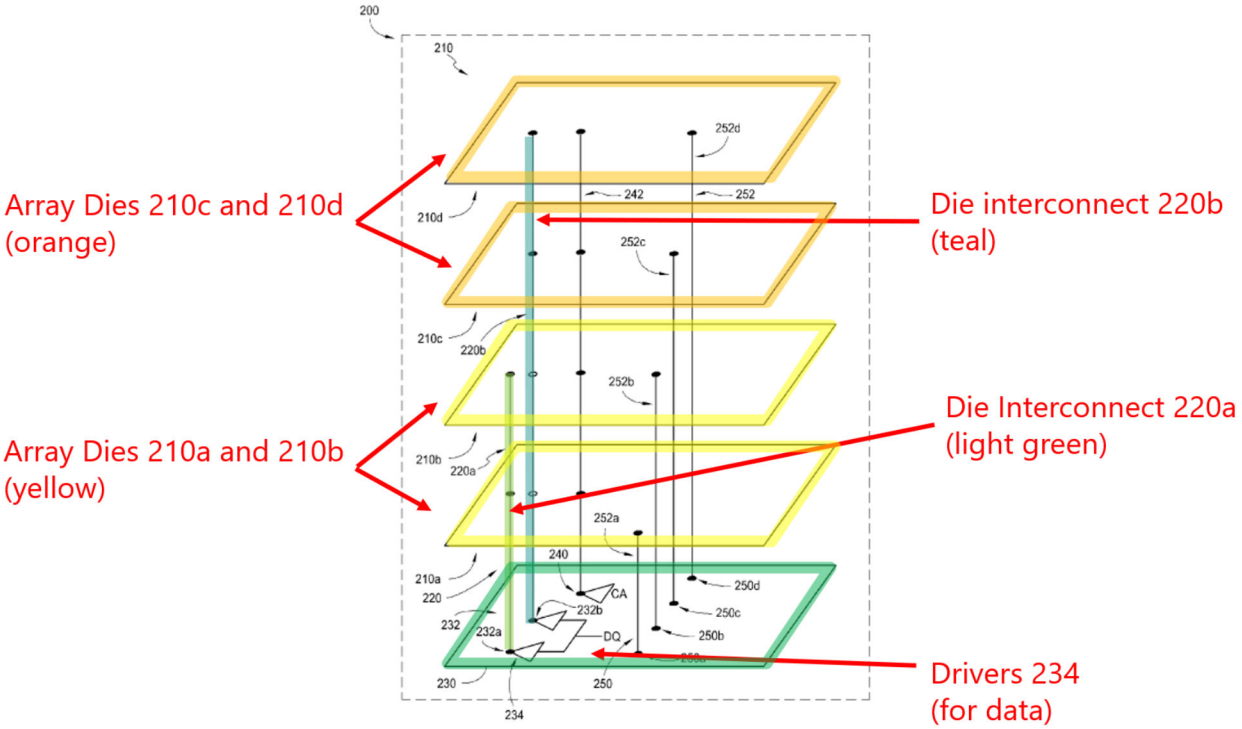


FIG. 2

32. In the example of Fig. 2, "die interconnect 220a [(light green)] may be in electrical communication with a data port from array die 210a [(yellow)] and a data port from array die 210b [(yellow)] (as illustrated by the darkened circles in FIG. 2) and not in electrical communication with any data ports from array die 210c [(orange)] or any data ports from array die 210d [(orange)]." '060 Patent at 5:63-6:1. The other "die interconnect 220b [(teal)] may be in electrical communication with a data port from array die 210c [(orange)] and a data port from array die 210d [(orange)] (as illustrated by the darkened circles in FIG. 2) (e.g., corresponding to the same data bit, e.g., D0) without being in electrical communication with any data ports from array die 210a [(yellow)] and array die 210b [(yellow)]… Despite not being in electrical communication with any data ports from array die 210a and 210b [(yellow)], in some implementations, the die interconnect 220b [(teal)] may pass through the array dies 210a and 210b [(yellow)] (as illustrated by the unfilled circles) e.g., through through-holes or vias of array dies 210a and 210b." *Id.* at 6:9-15.

B. '918 and '054 patents

33. The '918 and '054 patents describe a memory system 1010 that "can be coupled to a host computer system and can include a volatile memory subsystem 1030 [yellow], a non-volatile memory subsystem 1040 [green], and a controller 1062 [red] operatively coupled to the non-volatile memory subsystem 1040," as well as a "second power supply 1080" (blue) comprising either "capacitors" or a "battery" to supply power during a power failure, as shown in Figure 12 (below). *See* '918 patent, 21:16-20, 26:8-43.

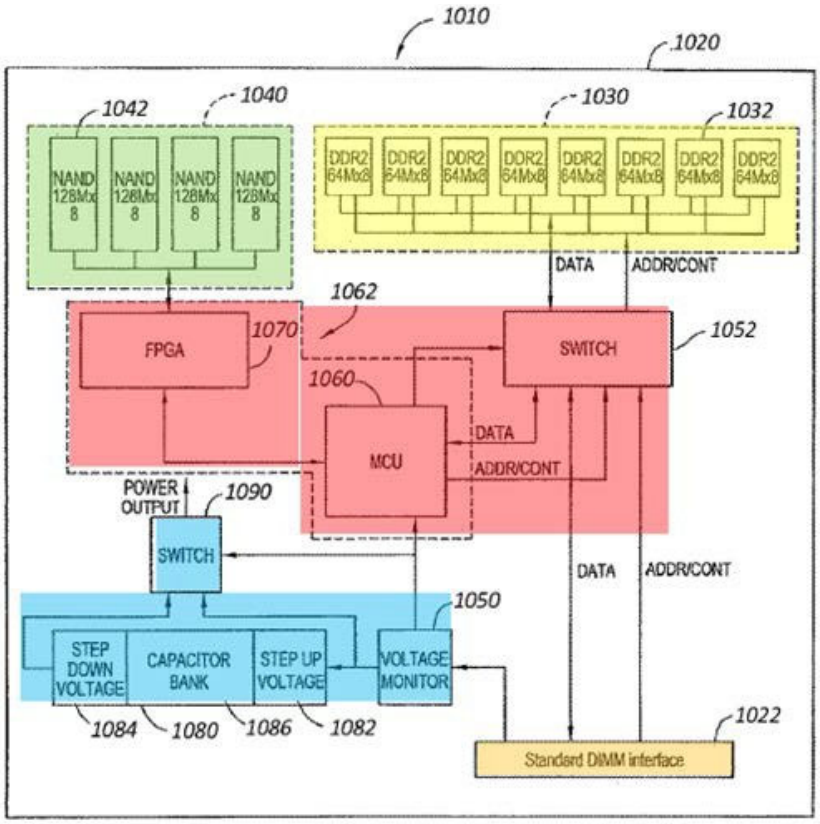


FIG. 12

34. In the event of a power failure detected by voltage monitor 1050, "[t]he controller [red] backs up the volatile memory [yellow] using the non-volatile memory [green]." '918 patent, 20:21-24, 25:8-27.

35. Figure 16 (below) illustrates a power module 1100 for the memory system above where "sub-block 1122 [below, right] comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter" which output four different voltages (1102=1.8V, 1104=2.5V, 1105=1.2V, 1107=3.3V) to the components of the memory system. '918 patent, 27:59-29:64.

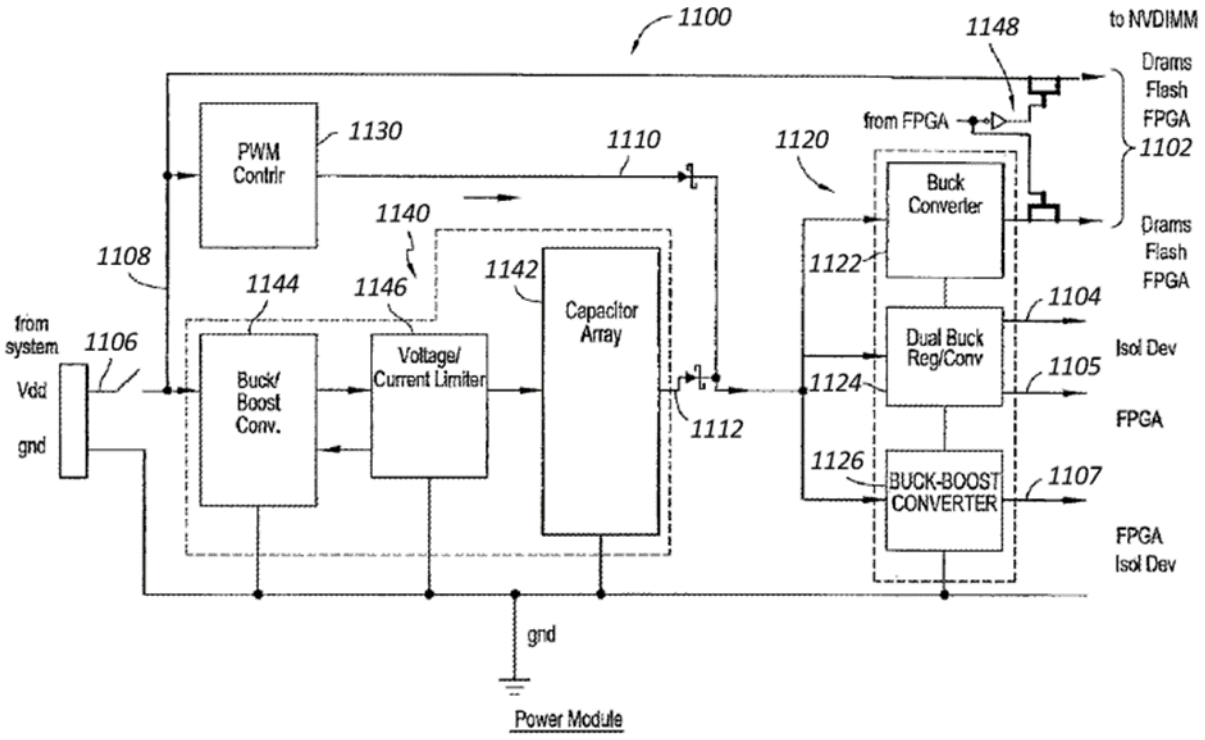


FIG. 16

VII. OPINIONS ON CLAIM CONSTRUCTION

A. '060 and '160 patents

1. "the second driver size being different from the first driver size" ('160 patent: all asserted claims)

36. I understand that the parties dispute the term "the second driver size being different from the first driver size," which appears in all asserted claims of the '160 Patent. For example, claims 1–2 of the '160 patent each include the disputed term:

1. A memory package, comprising:

data terminals and control terminals;

stacked array dies including a first group of array dies and a second group of at least one array die;

first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

a control die comprising first data conduits between the first die interconnects and the data terminals, and second data conduits between the second die interconnects and the data terminals, the first data conduit including first drivers each having a first ***driver size*** and configured to drive a data signal from a corresponding data terminal to the first group of array dies, the second data conduit including second drivers each having a second ***driver size*** and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second ***driver size*** being different from the first ***driver size***.

2. The memory package of claim 1, wherein the second die interconnects are longer than the first die interconnects, and wherein ***the second driver size is larger than the first driver size***.

37. I understand that the parties have proposed the below constructions for the disputed term:

Defendants' Proposed Construction	Netlist's Proposed Construction
The physical dimensions of the second driver being different from the physical dimensions of the first driver	the second driver size is different from the first driver size

38. Based on my analysis, and as I explain below, I agree with Micron's proposed construction.

39. Netlist's proposal substitutes in the claim language "being different" with "is different." I do not have an issue with that substitution but it does not address the core dispute between the parties, which is whether the term "driver size" should be interpreted according to its plain and ordinary meaning, i.e., physical dimensions of the driver, or should be expanded beyond its plain and ordinary meaning to include driver strength, which is distinct from driver size.

40. The language of the claims refer to the physical dimensions of the driver, as evidenced by the usage of the term "driver size" (claim 1) and whether one is "larger" than the other (dependent claim 2).

> 1. A memory package, comprising:
>
> data terminals and control terminals;
>
> stacked array dies including a first group of array dies and a second group of at least one array die;
>
> first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
>
> a control die comprising first data conduits between the first die interconnects and the data terminals, and second data conduits between the second die interconnects and the data terminals, the first data conduit including first drivers each having a first ***driver size*** and configured to drive a data signal from a corresponding data terminal to the first group of array dies, the second data conduit including second drivers each having a second ***driver size*** and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second ***driver size*** being different from the first ***driver size***.
>
> 2. The memory package of claim 1, wherein the second die interconnects are longer than the first die interconnects, and wherein ***the second driver size is larger than the first driver size***.

41. If the claims intended the refer to the strength of the driver, instead of its physical dimensions, then the claims simply could have used the term "driver strength." Instead, the applicant specifically chose to specify that the "driver size" must be different.

42. The specification further supports my view that the "driver size" refers to the physical dimensions of the driver such as the following portions of the specification below which refers to the amount of space a driver takes up on a die or the number of physical transistors directly relating to the size of the die.

> Generally, a load exists on each of the drivers 134, 140, 184, and 186 by virtue of the drivers being in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies. Thus, to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver. However, generally ***a larger driver not only consumes more space on the control die***, but also consumes more power.

'160 Patent at 2:10-17.

> As can be seen from Table 1, the maximum load of any conduit 332, using the example values previously described, is 3 L, or rather three times the load of a single array die 310. Assuming the same example values, the load of a conduit in electrical communication with a die interconnect that itself is in electrical communication with each array die 310 would be 10 L. Thus, certain embodiments of the present disclosure enable a reduction in the load of the conduits 332. Consequently, in some embodiments, the drivers 334 may each be smaller than a single driver that is configured to drive a signal from a conduit along a single die interconnect that is in electrical communication with a port from each of the array dies 310. Moreover, ***the drivers 334 may include smaller transistor sizes than a single driver that is configured to drive a signal to each of the array dies 110.***

'160 Patent at 13:13-26.

> The process **500** further comprises selecting a driver size for a first driver at block **508** and selecting a driver size for a second driver at block **510**. Selecting the driver size can be based, at least in part, on the calculated load on the driver. Generally, the greater the load on the driver, the larger the driver is selected to drive a signal along, for example, a die interconnect. ***The size of the driver may be adjusted by the selection of the transistor size and/or number of transistors included in the driver.*** A larger driver often consumes more power than a smaller driver. Thus, in certain embodiments, balancing the loads on the drivers to reduce the load on each driver can reduce the power consumption of a memory package.

'160 Patent at 17:14-25.

43. There is no description in the specification that explains that driver size can be changed by any way other than modifying its physical dimensions.

44. I understand that Netlist proposes that the term "driver size" could also refer to "driver strength" because Netlist contends that two drivers with the same physical dimensions could nevertheless drive different currents (which Netlist appears to frame as "logical size"). But a POSITA would have understood that driver size and driver strength are different engineering

concepts. For example, a POSITA would have understood that one could modify the physical dimensions of a driver without altering its drive strength. A POSITA would also have understood that one could modify the driver strength without modifying the physical dimensions of the driver. Thus, driver size and driver strength are distinct engineering concepts.

45. Using Metal Oxide Field Effect Transistors ("MOSFETs") as an example, the current that a MOSFET can drive in saturation mode, which is often utilized in drivers,[1] is expressed as follows:[2,3]

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

46. Here, I_D denotes the current that can be driven through a MOSFET; W and L denote the physical dimensions of the transistor channels and more specifically the channel width and length; and V_{GS} represents the voltage difference at the gate and source terminals of the transistor. In this example, one could double the channel width (W) and length (L) at the same time, which would alter the "driver size," but retain the same "driver strength" (I_D). Conversely, one could increase the "driver strength" (I_D) by increasing the voltage difference (V_{GS}) while maintaining the same "driver size" (W and L).

47. This is one of the examples that illustrate why "driver strength" and "driver size" are distinct concepts and thus why a POSITA would not have understood that having same/different "driver size" means or includes having same/different "driver strength."

[1] *See*, *e.g.*, https://www.ti.com/lit/ml/slua618a/slua618a.pdf at p. 11 (discussing advantages of using MOSFET transistors in drivers for high speed, high frequency switching applications).
[2] https://inst.eecs.berkeley.edu/~ee105/sp08/lectures/lecture16.pdf
[3] https://www.researchgate.net/profile/Nabil-Ashraf/post/How_to_extract_the_effective_channel_length_of_MOS_transistor/attachment/5d5fcdc43843b0b98260b5c6/AS%3A795023092240384%401566559684172/download/Extraction+of+MOSFET+Effective+channel+length+and+width.pdf

48. Therefore, it is my opinion that the term means "the physical dimensions of the second driver being different from the physical dimensions of the first driver."

B. '918 and '054 patents

1. "converter circuit"

49. I understand the parties have proposed the below constructions for this limitation.

'918 patent: all asserted claims	
Micron's Proposed Construction	**Netlist's Proposed Construction**
This is a means-plus-function limitation. **Functionality** • (i) "provid[ing] a fourth regulated voltage having a fourth voltage amplitude"; • (ii) "reduc[ing] the pre-regulated input voltage to provide a fourth regulated voltage"; • (iii) "provid[ing] the fourth regulated voltage"; and • (iv) "reduc[ing] the pre-regulated voltage input to provide the fourth regulated voltage." **Corresponding Structure** • The corresponding structure that is "configured to" perform the recited functions is a "converter circuit," as described in the '918 patent at 29:18–64.	A circuit for voltage conversion

50. I will refer to this limitation as the "converter circuit limitation."

51. I have reviewed the use of the term "converter circuit" in the asserted claims of the '918 patent. The use of "converter circuit" in the asserted claims provides no guidance of specific structure to a POSITA who would understand the term "converter circuit" in the asserted claims to be a generic term that encompasses any hardware, software, or combination that may perform the claimed functions of the converter circuit limitation of the asserted claims. In other words, the

claim term "converter circuit" does not inform a POSITA of the structural characteristics of the claimed "converter circuit" that is configured to perform the claimed functions of the converter circuit limitation of the asserted claims.

52. The remaining claim language of the converter circuit limitation includes functional language that does not inform a POSITA of any structural character of the "converter circuit." For example, the claims do not describe how the "converter circuit" interacts with other claimed components to perform the claimed functionality so as to inform a POSITA of the structural character of the term "converter circuit." Specifically, the remaining claim language specifies merely additional functions that the claimed "converter circuit" be configured to perform. None of this language, nor any other language in the claims of the '918 patent, provides any indication of a structure or category of structures narrowing the understanding of a POSITA that any hardware, software, or combination could be used to perform the claimed functions of the converter circuit limitation.

2. "at least one circuit"

53. I understand the parties have proposed the below constructions for this limitation.

'918 patent: claims 1-3, 5-7, 9-13, 15, and 21	
Micron's Proposed Construction	**Netlist's Proposed Construction**
This is a means-plus-function limitation. **Functionality** • (i) "receiv[ing] a first plurality of address and control signals via the first portion of the plurality of edge connections"; • (ii) "output[ting] a second plurality of address and control signals to the plurality of SDRAM devices"; • (iii) "receiv[ing] a first plurality of address and control signals via a second portion of the plurality of edge connections"; and	Plain and ordinary meaning

• (iv) "output a second plurality of address and control signals to the plurality of SDRAM devices." **Corresponding Structure** • The corresponding structure that is "operable to" perform the recited functions is a "circuit that is different from a memory module controller," as described in the '918 patent at 21:14–26:65, 29:33–54.	

54. I will refer to this limitation as the "at least one circuit limitation."

55. I have reviewed the use of the term "at least one circuit" in claims 1-3, 5-7, 9-13, 15, and 21 of the '918 patent. The use of "at least one circuit" in claims 1-3, 5-7, 9-13, 15, and 21 provides no guidance of specific structure to a POSITA who would understand the term "at least one circuit" in claims 1-3, 5-7, 9-13, 15, and 21 to be a generic term that encompasses any hardware, software, or combination that may perform the claimed functions of the at least one circuit limitation of claims 1-3, 5-7, 9-13, 15, and 21. In other words, the claim term "at least one circuit" does not inform a POSITA of the structural characteristics of the claimed "at least one circuit" that is configured to perform the claimed functions of the at least one circuit limitation of claims 1-3, 5-7, 9-13, 15, and 21.

56. The remaining claim language of the at least one circuit limitation includes functional language that does not inform a POSITA of any structural character of the "at least one circuit." For example, the claims do not describe how the "at least one circuit" interacts with other claimed components to perform the claimed functionality so as to inform a POSITA of the structural character of the term "at least one circuit." Specifically, the remaining claim language specifies merely additional functions that the claimed "at least one circuit" be configured to perform. None of this language, nor any other language in the claims of the '918 patent, provides

any indication of a structure or category of structures narrowing the understanding of a POSITA that any hardware, software, or combination could be used to perform the claimed functions of the at least one circuit limitation.

3. "controller"

57. I understand the parties have proposed the below constructions for this limitation.

'918 patent: claims 12, 18-19, and 25-26; '054 patent: claims 5, 7-13, 16-17, 23-25, and 29-30	
Micron's Proposed Construction	**Netlist's Proposed Construction**
This is a means-plus-function limitation. **<u>'918 patent</u>** **Functionality claimed in '918 patent** • (i) "receiv[ing] the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory"; • (ii) "receiv[ing] the signal, wherein the controller executes a write operation in response to the signal"; and • (iii) "receiv[ing] the signal, wherein, in response to the signal, the controller executes a write operation." **Corresponding structure in '918 patent** • The corresponding structure that is "configured to" perform the recited functions is a "controller that is different from the at least one circuit and the voltage monitor circuit and the one or more registers," as described in the '918 patent at 21:14–26:65, 29:33–54. **<u>'054 patent</u>** **Functionality claimed in '054 patent** • (i) "perform[ing] one or more operations including a write operation	Plain and ordinary meaning

to transfer data to non-volatile memory" "in response to the trigger signal"; and • (ii) "perform[ing] one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage, and wherein the one or more operations include a write operation to transfer data into non-volatile memory." **Corresponding structure in '054 patent** • The corresponding structure that is "configured to" perform the recited functions is a "controller that is different from the first circuit and the voltage monitor circuit," as described in the '054 patent at 21:14–26:65, 29:33–54.	

58. I will refer to this limitation as the "controller limitation."

59. I have reviewed the use of the term "controller" in claims 12, 18-19, and 25-26 of the '918 patent and claims 5, 7-13, 16-17, 23-25, and 29-30 of the '054 patent. The use of "controller" in those claims provides no guidance of specific structure to a POSITA who would understand the term "controller" in claims 12, 18-19, and 25-26 of the '918 patent and claims 5, 7-13, 16-17, 23-25, and 29-30 of the '054 patent to be a generic term that encompasses any hardware, software, or combination that may perform the claimed functions of the controller limitation of claims 12, 18-19, and 25-26 of the '918 patent and claims 5, 7-13, 16-17, 23-25, and 29-30 of the '054 patent. In other words, the claim term "controller" does not inform a POSITA of the structural characteristics of the claimed "controller" that is configured to perform the claimed functions of the controller limitation of claims 12, 18-19, and 25-26 of the '918 patent and claims 5, 7-13, 16-17, 23-25, and 29-30 of the '054 patent.

60. The remaining claim language of the controller limitation in the '918 patent and the '054 patent includes functional language that does not inform a POSITA of any structural character of the "controller." For example, the claims do not describe how the "controller" interacts with other claimed components to perform the claimed functionality so as to inform a POSITA of the structural character of the term "controller." Specifically, the remaining claim language specifies merely additional functions that the claimed "controller" be configured to perform. None of this language, nor any other language in the claims of the '918 patent and the '054 patent, provides any indication of a structure or category of structures narrowing the understanding of a POSITA that any hardware, software, or combination could be used to perform the claimed functions of the controller limitation.

VIII. CONCLUSION

For the reasons stated herein, a POSITA would have agreed with Micron's constructions for the disputed terms and phrases.

I hereby declare that the foregoing is true and correct to the best of my knowledge, subject to the laws of perjury of the United States.

DATED this 2nd day of May 2023.

Harold S. Stone

Dr. Harold S. Stone

Exhibit A

Curriculum Vitae

Harold S. Stone

Residence: 223 6th Ave., Kirkland WA 98033
Telephone: (609)-924-4780 [home and office, Princeton, NJ]
(732)-690-6728 [cell phone in WA and NJ]
Date of Birth: 10 August 1938
Place of Birth: St. Louis, Missouri
Citizenship: US

Education

Princeton	1956-1960	BSE	EE
Univ. of California, Berkeley	1960-1961	MSE	EE
Univ. of California, Berkeley	1961-1963	Ph. D.	EE

Awards and Honors.

Summa Cum Laude, Princeton, 1960
Whiton Scholarship, Princeton, 1958-1959
Phi Beta Kappa, Princeton, 1960
Sigma Xi, Princeton, 1960
Sigma Xi Book Award, Princeton, 1960
Bigelow Prize, Princeton, 1960
NSF Fellow, University of California, 1960-1963
Distinguished Visitor, IEEE Computer Society, 1971-1973, 1979-1980.
ACM National Lecturer, 1973-1975
Tau Beta Pi, U of Massachusetts, 1981
IEEE Fellow, 1986.
Charles Babbage Award, 1991. Citation: "In recognition of his exceptional contributions to the evolution of computer architecture and high performance computing."
Best Paper in Track, ICCD, 1992.
IEEE Emanuel Piore Award, 1992. Citation: "For fundamental contributions to parallel computer technology, and to computer science education."
ACM Fellow, 1994.
IEEE Computer Society Taylor Booth Education Award, 1999. Citation: "for outstanding contributions in advancing computer science and engineering education through your research, teaching and most important through innovative writing of seminal textbooks that established the computer architecture on a firm foundation. "

Areas of Research Activities

Image Data Bases, Image Registration, and Image Searching
Optical interconnections for computer systems
Computer Architecture
Distributed Processing
Image Processing
Parallel Algorithms
Microprocessor Systems
Operating Systems

Combinatorial Algorithms
Computer-aided Design of VLSI Networks

Positions Held

Fellow, NEC Research Institute, 8/94 - 4/01 (retired).
Research Staff Member, IBM, 1/90 to 7/94.
Manager, Advanced Architecture Studies, IBM, 9/84 to 1/90.
Adjunct Professor, Courant Institute of Mathematics, 1/85 to 6/90.
Professor, Electrical and Computer Engineering Department, University of Massachusetts, 9/74 to 8/84.
Associate Professor of Computer Science and Electrical Engineering, Stanford University, 9/70 to 8/74.
Acting Associate Professor of Computer Science and Electrical Engineering, Stanford University, 10/68-6/69 and 10/69-6/70. (On leave from SRI International.)
Research Engineer, SRI International, Menlo Park, California, 11/63-12/68.
Research Engineer, Boeing, Seattle, Washington, 7/63-11/63.

Visiting Positions

Visiting Professor, Cornell University, Electrical Engineering Department, 1992-1993.
Guest Lecturer in Computer Architecture, Ecole Polytechnique Federal de Lausanne, 10/91.
Guest Lecture Series, Electrotechnical Laboratory, Tsukuba, Japan, 12/87.
Visiting Lecturer, IBM Japan, 7/82-8/82.
Visiting Professor, University of California, Berkeley, California, 9/77-6/78.
Visiting Professor, University of Sao Paulo, Sao Paulo, Brazil, 7/75-8/75.
Guest Lecturer, IRIA, Paris, France, 6/74.
Visiting Scientist, Institute for Computer Applications in Science and Engineering, NASA Langley Research Center, Hampton, VA, 6/74-6/79.
NASA Visiting Research Fellow, NASA Ames Research Center, Mt. View, California, 9/73-6/74.
Guest Lecturer, Technical University of Berlin, 6/73-7/73.
OAS Lecturer, Universidad de Chile, Santiago, Chile, 7/72-8/72.
NASA ASEE Fellow, NASA Ames Research Center, Mt. View, CA, 6/71-9/71.
Lecturer in Communications, IBM, San Jose, CA, 6/66-7/66.

Consultantships

Expert Consultant, Winston-Strawn, 7/21 to present
Expert Consultant, Finnegan-Henderson, 1/21 to present
Expert Consultant, Haynes-Boone, Law firm; 4/16 to 12/20, testifying in IPR cases IPR2016-00924, IPR2016-00925, HTC and Apple v. PUMA, testifying for Apple.
Expert Consultant, Winston and Strawn, Law firm, 2/16 to 6/16, testifying in 2:14-cv-689-JRG-RSP, PUMA v. HTC et al, testifying for Motorola.
Expert Consultant, Sidley-Austin, Law firm, 4/15 to 12/20, testifying in 2:14-cv-690- RSP, PUMA v. HTC et al, testifying for HTC; IPR cases IPR2015-01500, IPR2015-01501, IPR2015-01502, HTC et al v. PUMA, testifying for HTC; IPR cases IPR2016-00924, IPR2016-00925, HTC and Apple v. PUMA, testifying for HTC; IPR cases IPR2017-00549, IPR2017-00577, IPR2017-00667, IPR2017-00668, IPR2018-00362, and IPR 2018-00363, SK hynix v. Netlist, testifying for SK hynix; IPR cases IPR2018-01594, IPR2018-01601, IPR2018-01602, IPR2018-01603, IPR2018-01605, IPR2018-01606, and IPR2018-1607,

Microsoft v. St. Regis Tribe (later changed to Microsoft v DirectStream), testifying for Microsoft.

Expert Consultant, Paul Hastings, Law firm, 5/15 to 3/16, testifying in 2:14-cv-687-JRG-RSP, PUMA v. Samsung et al, testifying for Samsung; and IPR cases IPR2015-01500, IPR2015-01501, IPR2015-01502, HTC et al v. PUMA, testifying for Samsung.

Expert Consultant, Fish and Richardson Law firm. 7/15 to 8/15.

Expert Consultant, Nelson, Bumgardner, and Casto, law firm; 5/11 to 3/14, testifying in Stragent V. Intel. Civil Action no. 6:11-CV-421.(testified on behalf of Stragent)

Expert Consultant, Devlin Law Firm, 8/14 to 10/14.

Expert Consultant, Finnegan-Henderson, 8/10 to 12/16, testified in TSC v. Mountcastle, et al., No. 1:10-cv-00901-TSE-TC. (testified on behalf of TSC), testifying in Parthenon Unified Memory Architecture v. LG et al. (also representing HTC, Samsung, Huawei, Motorola Mobility, ZTE, and Apple codefendants represented by other law firms), PUMA v. LG, HTC, and Samsung in Inter Partes Reviews IPR2015-01494, IPR2015-01500, IPR2015-01501, IPR2015-01502, IPR2015-01944, and IPR2015-01946 (testified on behalf of LG, HTC, and Samsung), IPR case to be assigned, (testified on behalf of Apple), IPR case to be assigned (testified on behalf of ZTE) testifying in PUMA v. HTC ,Case No. 2:14-cv-00690-RSP in (testifying on behalf of HTC), testifying in PUMA v. LG, Case No. 2:14-cv-00691-JRG-RSP (testifying on behalf of LG), testifying in PUMA v. ZTE, Case No. 2:15-cv-00225-JRG-RSP (testifying on behalf of ZTE)

Expert Consultant, Nix, Patterson, and Roach, 12/11 to 3/12.

Expert Consultant, Barcelo, Harrison, and Walker, 12/11 to 15/1.

Expert Consultant, Irell and Manella, 12/11 to 5/12.

Expert Consultant, Williams, Morgan, and Amerson, 1/11 to 3/12

Expert Consultant, Perkins-Coie, 5/10 to 5/11.

Expert Consultant, Quinn Emanuel, 10/10 to 4/13, testifying in Microunity v. Apple et al., No. 02:10-cv-91-LED-RSP (testified on behalf of Qualcomm, LG, HTC, and Google)

Expert Consultant, Alston and Bird, 12/09 to 5/12, testifying in AIT v. Dell, No. 5:07 CV 426-H (testified on behalf of Dell).

Expert Consultant, Irell and Manella, 11/08-11/09, testifying in WARF v. Intel, 3:08-cv-00078-bbc (W.D. Wisc), (testified on behalf of WARF).

Expert Consultant, Bartlit Beck Herman Palenchar and Scott, 11/07 to 12/12, testifying in Convolve/MIT v. Seagate/Compaq, No. 00 CIV 5141 (GBD) (testified on behalf of Compaq).

Expert Consultant, Williams, Morgan, and Amerson, 11/06 to 11/08, testifying in BIAX v. Fujitsu and Sun Microsystems, No. 2:06-CV-364-TJW (testified on behalf of BIAX).

Expert Consultant, Ropes and Gray, 9/06 to 11/07, testifying in Convolve/MIT v. Seagate/Compaq, No. 00 CIV 5141 (GBD) (testified on behalf of Compaq)..

Consulting Editor for Prentice-Hall Publishing, 1999 to 2010.

Consultant, Los Alamos National Laboratory, NIS Division, 12/01 to 1/04; ISR Division, 1/04 to 2006; N Division, 1/04 to 2005.

Expert Consultant, McDermott, Will, and Emery, 11/05 to 2/07, testifying in BIAX v. Philips, No. 337-TA-559 (ITC) (testified on behalf of BIAX).

Expert Consultant, Finnegan Henderson Farabow Garrett and Dunner, 3/05 to 4/09, testifying in Biax v. Intel and ADI, No. 02-05-CV-184-TJW (E.D. Tex) (testified on behalf of BIAX, in Lofgren v. Prutchi, Patent Interference No. 105,581 (JL), (Technology Center 2800) (testified on behalf of Prutchi (Boston Scientific)), in Paradox v. ADT/DSC, No. 2:06-CV-00462-TJW (E.D. Tex) (testified on behalf of DSC, in BIAX v. Analog Devices, AAA Matter No. 11 181 Y 00186 09 (testified on behalf of BIAX)**;** and author of declaration in Reexamination of US Patent 5,077,733 to Whipple, docket 04747.0177-00; 8/10 to 9/12,

testifying in Biax v. Motorola Solutions, Inc et al., Civil Action No. 10-cv-03013-PAB-KLM (testified on behalf of Biax). 6/11 to 8/12, testifying in VIA *et al*. v. Apple before the ITC, action 337-TA-812 (testified on behalf of VIA),.

Expert Consultant, Weil, Gotshal, and Manges, 1/03 to 5/04, testifying in Mangosoft, Inc. v. Oracle Corp., No. 02-545-JM (D.N.H.) (testified on behalf of Oracle).

Expert Consultant, Amster, Rothstein, and Ebenstein, 8/03 to 12/06.

Expert Consultant, Irell and Manella, 2/03 to 1/05.

Expert Consultant, Howrey, Simon, 8/02 to 1/07.

Consultant, NASA Goddard Space Flight Systems, 4/01 to 12/04.

Expert Witness, Fish and Neave, 1/02 to 4/03, testifying in Intel Corp v. Via Tech, No. A-01-CA602-SS (W.D. Tex.) (testified on behalf of Via Tech).

Consulting Editor for PWS Publishing Series in Computer Architecture, 1993-1999.

Consulting Editor for Addison/Wesley Series in Microcomputers, 1983-1992.

Consultant, IBM Watson Research Center, 9/83-8/84.

Consultant, Unidata Systems, Inc., 6/82-6/84.

Consultant, Sperry Systems Management, Great Neck, NY, 6/82-8/84.

Consultant, Assurance Technology, Carlisle, MA, 6/82-8/84.

Consultant, IBM Federal Systems Division, 5/83-6/83.

Consultant, IBM Watson Research Center, 1/82-5/82.

Member of Advisory Committee, Solo Systems, Sunnyvale, CA, 4/82.

Consultant, IBM Federal Systems Division, 8/81-9/81.

Consultant, Assurance Technology, Carlisle, MA, 4/81-12/81.

Consultant, Sky Computer, Lowell, MA, 4/81-6/81.

Consulting Editor, University Microfilms, 12/80-12/85.

Consulting Researcher, Sperry Research Center, Sudbury, MA, 6/80-2/81.

Consultant, Sperry Systems Management, Great Neck, NY, 4/80-1/82.

Consultant, Gartner Group, Greenwich, CT, 5/80-6/81.

Consultant, Georgia Institute of Technology Engineering Station, 1/80 to 6/80.

Consultant, GTE Sylvania, Needham Heights, MA, 7/79.

Consultant, The Analytic Sciences Corporation, Reading MA, 7/79.

Consulting Editor and Series Editor, McGraw-Hill, 1978-12/83.

Consultant, Dean-Witter Reynolds, New York, 1978-1979.

Consultant, Douglas Peterson and Assoc., Greenfield, MA, 1978-1981.

Consultant, Monolithic Memories, Sunnyvale, CA, Inc., 1978

Consultant, GE Naval Ordnance Systems, Pittsfield MA, 1977.

Consultant, US Army CORADCOM, Fort Monmouth, NJ, 1975-1980.

Consultant, Imagetics, Inc., Greenfield, MA, 1975-1977

Member of Advisory Committee, Hewlett-Packard, 1975-1976.

Consultant, Hewlett-Packard, 1970-1974, and 1975-1978.

Consultant, Systems Control, Inc., Palo Alto, CA 1970-1973 and 1975-1977.

Consultant, Bell Laboratories, 1974

Consultant, Wolf Mangagement Services (now Systems Control, Inc.), 1969-1970.

Consultant, SRI International, Menlo Park, CA, 1968-1969.

Consultant, Precision Instruments, Palo Alto, CA, 1968.

Consultant, Data Technology Corporation, Mt. View, CA, 1967-1970.

Consultant, RAND Corporation, Santa Monica, CA, 1962-1963.

Professional Societies

IEEE

ACM

SPIE

Professional Activities

Session Organizer, 2000 Conference on Information Sciences and Systems, March, 2000
Member, NSF Panel, Next Generation Software Panel, 1999
Guest Co-Editor, IEEE Communications Magazine, January 1999
Member, Program Committee, 1999 Workshop on High-Speed Interconnections with Digital Computers
Member, Program Committee, Conference on Applications for Digital Libaries, 1995-1999
Member, Program Committee, 1998 International Super Computer Symposium
Member, Program Committee, 1998 ICCV Workshop on Content-Based Access of Image/Video Library Data
Speaker and Participant, 1998 NIH Lung Imaging Workshop on Technology Transfer
Member, Program Committee for 1997 Image Registration Workshop
Member, IEEE Awards Committee (Corporate Recognition and Best Papers), 1996-2000
Member, NSF Panel, Opportunities for Multidisciplinary Research, 1995
Chair, Science Council, Center of Excellence in Space Data and Information Sciences, 1995-1997.
Chair, Search Committee for Director of Center of Excellence in Space Data and Information Sciences, 1994.
Member, National Research Council, ONR Panel for Computer Science, 1994.
Member, NSF Committee of Visitors, Computer and Computing Research, 1993.
Program Committee Organizer, Workshop on Interconnections within High-Speed Digital Systems, 1993.
Member, NSF Research Infrastucture Awards Panel, 1993.
Member, IEEE Fellows Selection Committee, 1992-1995.
Member, Science Council, Center of Excellence in Space Data and Information Sciences, 1992-1994.
Vice President, Publications, IEEE Computer Society, 1992.
Session Organizer, Workshop on Interconnections within High-Speed Digital Systems, 1992.
Member, NSF Presidential Faculty Award Selection Committee, 1992.
Chair, Transactions Advisory Committee, IEEE Computer Society, 1991
Session Organizer, Workshop on Interconnections within High-Speed Digital Systems, 1991
Member, NSF Presidential Young Investigator Selection Committee, 1991.
Program Chair, Workshop on Interconnections within High-Speed Digital Systems, 1990
Track Chair, ACM Critical Issues Conference, 1990
Member, IEEE Hamming Award Selection Committee, 1990
Chair, Audit Committee, Computer Society Governing Board, 1989-90.
Member, IEEE Computer Society Governing Board, 1986-1992
Associate Editor, *IEEE Transactions on Parallel and Distributed Systems*, 1989-1993
Chair, Technical Committee on Interconnections within High-Speed Digital Systems, 1989-1990
Chair, IEEE Tab Awards and Recognition Committee, 1990
Member, NSF PYI Selection Panel, 1989, 1991
Member, Marist College Computer Selection Advisory Committee, 1988-1989
Member, ACM/IEEE Eckert-Mauchly Award Committee, 1988-1990.
Member, IEEE Tab Awards Committee, 1989
Member, IEEE Fellows Committee, Computer Society Representative, 1988-1990.
Chair, IEEE Kobayashi Field Award, 1987-1989.
Member Audit Committee, Computer Society Governing Board, 1988.

NSF Site Review Committee, Engineering Research Center Selection, 1988.
Member, NSF Coordinated Equipment for Research Selection Panel, Feb. 1986, Feb. 1987.
Member, Dartmouth College Advisory Committee, 1986-1987.
Member, NSF Presidential Young Investigator Panel, 1985
Member, NSF Advisory Committee, Manufacturing, Design, and Computer Engineering, 1985-1986
Member Visiting Committee, University of Texas, Electrical and Computer Engineering Department, 1985-1986.
Member, NSF Research Initiation Grant Selection Panel, 1985.
Program Chairman, 1986 Fall Joint Computer Conference
North American Conference Chairman, 13th Annual Computer Architecture Symposium, 1986.
Panelist, Review of ONR funding of Artificial Intelligence Research, National Academy of Science, 1985-1986.
Co-Chair and Author, IEEE Task Report on Research Priorities in Computer and Communication Research, 1985.
Program Committee Member, International Conference on Computers and Applications, Peking, China, 6/84.
Panelist, Study on International Developments, National Academy of Science, 1/83-12/85.
Panelist, Study on Chemical and Biological Sensor Technology, National Academy of Science, 4/83-1/84.
Panel Chairman, Distributed Systems Research, NSF Workshop on Future Directions in Computer Research, 1/83.
Member, Advisory Panel on Computer Engineering, National Science Foundation, 1981-1983.
Editorial Board, Proceedings of the IEEE, 2/81-12/84.
Member, Computer Science Board, National Academy of Sciences, 1979-1984.
Panelist, Study in Research Paradigms of Computer Science, National Academy of Sciences, 1980-1982.
Panelist, NSF Workshop on Future Directions of Computer Engineering Research, 11/81.
Member, and coauthor of proposal accepted by, IEEE Computer Society Floating-Point Standardization Committee, 1978-1982.
Session Organizer and Session Chairman, Electro '80, May 1980.
Guest Editor, Issue on Military Computer Family Architecture, *Computer*, April 1979.
Chairman, Eckert-Mauchly Award Committee, IEEE CS and ACM, 1979-1981
Member, Awards Committee, IEEE Computer Society, 1980-1981
Member, Governing Board, IEEE Computer Society, 1979-1980. Advisor, IEEE Computer Society, Computer Tutorial Series, 1978.
Program Committee, Sixth Annual Computer Architecture Symposium, April 1978.
Program Committee, Fifth Annual Computer Architecture Symposium, April 1977.
ECDP Accreditation Team visitor, 1976.
Member, IEEE Piore Award Committee, 1976-1978.
Editorial Board, *J. ACM*, 1976 to 1980.
Workshop Committee, Distributed Processing Workshop, Brown University, August 1976.
Program Chairman, Fourth Annual Computer Architecture Symposium, April 1977.
Chairman, Hardware Systems Panel, Computer Science and Engineering. Research Study (COSERS), 1974-1976.
Member, Advisory Panel on Computer Science and Engineering, National Science Foundation, 1974-1977.
Program Committee, Sagamore Conference on Parallel Computation, August 1973.
Program Committee, Second Annual Symposium on Computer Architecture, January 1975.
Program Committee, First Annual Symposium on Computer Architecture, December 1973.

Program Committee, Symposium on Sequential and Parallel Numerical Algorithms, May 1973.
Guest Editor, Special Issue on Parallel Computation, *IEEE Trans. on Computers*, August 1973.
Board of Directors, SIGARCH, ACM, 1974-1976.
Chairman, Technical Committee on Computer Architecture, IEEE Computer Society, 1972-1973.
Workshop Chairman, Parallel Computation Workshop, June 1972.
Chairman, Best Papers Awards Committee, IEEE Computer Society, 1974 to 1977.
Member, Governing Board, IEEE Computer Society, 1973-1974.
Chairman, San Francisco Chapter, IEEE Computer Society, 1972-1973.
Vice-Chairman, San Francisco Chapter, IEEE Computer Society, 1971-1972.
Technical Editor, *Computer*, IEEE Computer Society, 1971-1973.
Review Editor, *IEEE Computer Transactions*, 1966-1969.

Editor and Reviewer of Manuscripts

500 manuscripts reviewed, 1970-1995 for:
- Addison-Wesley
- Allyn and Bacon
- John Wiley and Sons
- Mayfield Press
- McGraw-Hill
- MacMillan
- Prentice Hall
- Prindle, Webster, and Smith
- Science Research Associates
- Springer Verlag

Consulting Editor for PWS
- 1 book in the series

Consulting Editor for McGraw-Hill Computer Science Series
- 14 books in the series

Consulting Editor for University Microfilms Series in
- Artificial Intelligence
- Distributed and Data Base Systems
- Systems Programming
- Computer Architecture
  - 76 books in the series

Consulting Editor for Addison-Wesley
- 5 books in the series

Directorships and Corporate Affiliations.

Director, EZ Data Systems, Newington, NH, 1981-1983
President and Director of The Interfactor, Inc., 1980-1993

Bibliographical Information

Books and Book Chapters

1. *Image Registration for Remote Sensing*, J. LeMoigne, *et al.*, eds, Cambridge University Press, 2011. (One chapter by H. S. Stone, co-author of two other chapters).
2. Stone, H. S., "Content-based image retrieval — Research issues," Chapter 9 of *Recent Advances in Multimedia*, B. Sheu and M. Ismail, editors, IEEE Press, pp. 282-322, 1998

3. Stone, H. S., *High-Performance Computer Architecture*, Addison-Wesley, Reading MA, 1987. Second edition, 1990. Third edition, 1993.
4. Stone, H. S., *Microcomputer Interfacing*, Addison-Wesley, Reading MA, 1982.
5. *Introduction to Computer Architecture*, Harold S. Stone, ed., Science Research Associates, Palo Alto, 1975. 2nd Edition, 1980. (Two chapters by Harold S. Stone).
6. Stone, H. S., and D. P. Siewiorek, *Introduction to Computer Organization and Data Structures, PDP-11 Edition*, McGraw-Hill, New York, 1975.
7. Stone, H. S., *Discrete Mathematical Structures and Their Applications*, Science Research Associates, Palo Alto, 1973.
8. Stone, H. S., *Introduction to Computer Organization and Data Structures*, McGraw-Hill, New York, 1972.
9. *Recent Advances in Switching Theory*, A. Mukhopadhyay, ed., Academic Press, New York, 1971. (Two chapters by H. S. Stone)

Patents

1. Natarajan, K. S., and H. S. Stone, "Adaptive mechanisms for execution of sequential decisions," US Patent 4,752,890, 21 June 1988.
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Sample of Invited Talks

1. Keynote Speech, ICCD '96, Austin Texas, October 1996.
2. Keynote Speech, Workshop on High-Speed Interconnections within Digital Systems, Santa Fe, New Mexico, May, 1996.
3. Stone, H. S., "Fourier domain techniques for image querying," Centre for Advanced Studies Conference, Toronto, November, 1995.
4. Stone, H. S., "Pattern matching of remote-sensing data," Tutorial in CESDIS Distinguished Lecture Series, October, 1995.
5. Keynote Speech, "Image processing and its impact on computer architecture", 1995 High-Performance Computer Architecture Symposium, March, 1995, and at Santa Fe Workshop on High-Speed Interconnections within Digital Systems, May, 1995.